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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,512	10/01/2003	Woo Sik Yoo	M-15121 US	8239

7590 08/25/2004

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,512	YOO, WOO SIK	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/1/03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 10/01/03. Currently, claims 1-15 are pending.

Drawings

The drawings are objected to because: Figures 1A-1F should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: On page 5, paragraph [0133], line 5, and page 6, paragraph [0138], line 6, the Examiner requests clarification with regards to, as stated "surface 304" and "SOI active layer 304", respectively, the reference number "304" identifies two completely different parts with regards to figure 3. For examination purposes, the Examiner will regard this as "surface 304". Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura US Patent 6,211,041 in view of Sakaguchi et al. US Patent 6,313,014.

Ogura shows the semiconductor method substantially as claimed. See figures 1A-2F, and corresponding text, pertaining to claims 1 and 9, Ogura shows a method for forming a SOI structure, comprising: providing a silicon (first) substrate **1** (figure 1A) and a support (second) substrate **2** (figure 1A); applying a layer of SiO_2 **3** (figure 1B; col. 1, lines 38-39) to said first substrate **1**; implanting an impurity through said SiO_2 into said silicon (first) substrate to a first depth **4** (figure 1C; col. 1, lines 44-47); bonding said silicon (first) substrate to said support (second) substrate with said layer of SiO_2 disposed therebetween (figure 1D; col. 1, lines 59-64); and heating the first depth of said silicon substrate to an annealing temperature (col.1, lines 64-67; col. 2, lines 1-7). In addition, Ogura shows, pertaining to claims 4 and 12, the method, wherein said support (second) substrate comprises quartz (col. 4, lines 38-40). Ogura also shows, pertaining to claims 7 and 15, the method, wherein said annealing temperature is between about 500°C and 1400°C (col. 2, lines 16-17 and lines 39-41). Finally, Ogura shows, the method, pertaining to claim 13, wherein said second substrate comprises SiC, GaAs, GaP, InP, GaN, and Al_2O_3 (col. 4, lines 38-40).

However, Ogura fails to show, pertaining to claims 1 and 9, a method for forming an SOI structure, with flashing said support substrate with radiation energy which impinges on a surface of said support substrate for a substantially instantaneous time to go through said support substrate and heat the first depth of said silicon substrate to an annealing temperature. In addition, Ogura fails to show, pertaining to claims 2 and 10, wherein said radiation energy is derived from a radiation energy source comprising a high-intensity lamp, and that flashing comprises energizing a high-intensity lamp for a substantially instantaneous time. Also, Ogura fails to show, pertaining to claim 3, wherein said high-intensity lamp comprises a Xe arc lamp. Ogura fails to show, pertaining to claim 5, wherein said radiation energy comprises an average power of between about 0.5 J/cm^2 and about 100 Jcm^2. Ogura fails to show, pertaining to claims 6 and 14, wherein said first depth comprises a portion of said silicon substrate between 10 nm and about 1 mm below a surface of said silicon substrate. Finally, Ogura fails to show, pertaining to claims 8 and 11, wherein said substantially instantaneous time is between about 1 nanosecond and about 10 seconds.

Sakaguchi teaches in figures 1-11C, and corresponding text, a method for manufacturing a SOI substrate, pertaining to claims 1-3, and 9, using an annealing process, that utilizes radiation of a lamp for the purpose of Rapid Thermal Annealing (RTA) as an alternative to conventional heat treatment, that includes the use of a flash annealing apparatus using a xenon flash lamp for several seconds to several hours (col. 8, lines 21-35). The annealing process also reduces unwanted inherent defects in the SOI wafer.

It would have been obvious to one of ordinary skill in the art to have incorporated, substituting flashing the support substrate with a radiation energy, where the radiation energy source is a high-intensity lamp and includes a Xe arc lamp, that impinges on a surface of the support substrate for a substantially instantaneous time to go through the support substrate, and heats the first depth of the silicon substrate to an annealing temperature, in the method of Ogura, pertaining to claims 1-3, 9 and 10, according to the teachings of Sakaguchi, with the motivation that, as stated in col. 8, lines 25-35, the Rapid Thermal Annealing process, includes the use of a flashing annealing apparatus, using a xenon flash lamp, where one of ordinary skill in the art would be drawn to use this process as an alternative to conventional annealing process, since conventional RTA processes are well known for their fast-ramp thermal processing capabilities and since the RTA process in Sakaguchi reduces inherent defects in the SOI wafer. Therefore, by including this RTA process, the support substrate will experience smaller amounts of thermal exposure that will result in reduced stress and damage to the substrate, due to reduced excessive heat exposure, and reduced processing time. Finally, radiating the energy source using flash annealing to impinge on a surface of the support substrate, for a substantially instantaneous time, to go through the support substrate, and to heat the first depth of silicon substrate, will ultimately be accomplished since the hydrogen ions are exposed to a relatively high temperature, due to the use of the RTA process.

It would have been obvious to one of ordinary skill in the art to have incorporated the radiation energy comprising an average power of between about 0.5 J/cm^2 and about 100 J/cm^2; the first depth of the silicon substrate being between 10 nm and about 1mm below the surface of the silicon substrate; and the instantaneous time being between

about 1 nanosecond and about 10 seconds, in the method of Ogura, pertaining to claims 5, 6, 8, and 14, based on the combined teachings of Ogura in view of Sakaguchi, with the motivation that, both methods are performed under the use of conventional techniques, resulting in the formation of an SOI substrate with reduced defects in the SOI active layer and substrate. Pertaining to claims 6, and 14, specifically, Ogura shows that the hydrogen ions are implanted within a certain depth with the motivation that the implanted hydrogen ions are used to break bonds between silicon atoms in the silicon crystal, and terminate non-bonded hands of the atoms. Therefore, the claimed first depth between 10 nm and about 1mm below the surface of the silicon substrate would be considered to be within conventional specifications for the hydrogen implant to accomplish this bond breaking and termination of non-bonded hands of the atoms since the bonds and hands are throughout the surfaces of the substrate, especially since no criticality has been shown. Pertaining to claims 5, and 8, specifically, Sakaguchi teaches that annealing an SOI wafer may be performed conventionally by Rapid Thermal Annealing (RTA) for a few seconds to several hours (col. 8, lines 33-35), as a result, the average power between 0.5 J/cm^2 and about 100 J/cm^2 and the instantaneous time between about 1 nanosecond and about 10 seconds are within conventional power specifications to accomplish the annealing process for a few seconds to several hours, especially since no criticality has been shown.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
August 21, 2004

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